ISL70001SRH, ISL70001SEH SPICE Average Model

Abstract

This application note describes how to use the SPICE model for the ISL70001SRH, ISL70001SEH Radiation Hardened and SEE Hardened 6A Synchronous Buck Regulator. This SPICE model was developed to help system designers evaluate the operation of this IC prior or in conjunction with prototyping a system design. This model accurately simulates typical performance characteristics at room temperature (+25°C) such as loop analysis, transient analysis and start-up. Functionality has been tested on CADENCE ORCAD 16.3. Other SPICE simulators may be used, however, the model may require translation.

Table of Contents

List of Figures

Introduction

The ISL70001SRH, ISL70001SEH are radiation hardened and SEE hardened high efficiency monolithic synchronous buck regulators with integrated MOSFETs, which operate over an input voltage range of 3.0V to 5.5V. Utilizing peak current-mode control with integrated compensation and a switching frequency of 1MHz, this Point-of-Load (POL) provides excellent dynamic response in a small form factor. High integration and class leading radiation tolerance makes the ISL70001SRH, ISL70001SEH the ideal POL solution for many space applications.

Reference Documents

- ISL70001SEH, ISL70001SRH Datasheet
- SMD 5962-09225

License Statement

The information in this SPICE model is protected under the United States copyright laws. Intersil Corporation hereby grants users of this macro-model hereto referred to as “Licensee”, a nonexclusive, nontransferable license to use this model as long as the Licensee abides by the terms of this agreement. Before using this macro-model, the Licensee should read this license. If the Licensee does not accept these terms, permission to use the model is not granted.

The Licensee may not sell, loan, rent, or license the macro-model, in whole, in part, or in modified form, to anyone outside the Licensee’s company. The Licensee may modify the macro-model to suit his/her specific applications, and the Licensee may make copies of this macro-model for use within their company only.

This macro-model is provided “AS IS, WHERE IS, AND WITH NO WARRANTY OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING, BUT NOT LIMITED TO, ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE.”

In no event will Intersil be liable for special, collateral, incidental, or consequential damages in connection with or arising out of the use of this macro-model. Intersil reserves the right to make changes to the product and the macro-model without prior notice.

Project Files

The zip file: **isl70001srh-pspice-average-model.zip** contains the project file ISL70001SRH.opj to be used in an ORCAD simulator. The project file has the model definition file (.lib), symbol file (.olb) and the schematic page as shown in Figure 1. Three simulation profiles are included in the project to simulate start-up, loop analysis and transient response. Figures 2 through 4 show the results of the three preset simulation profiles.

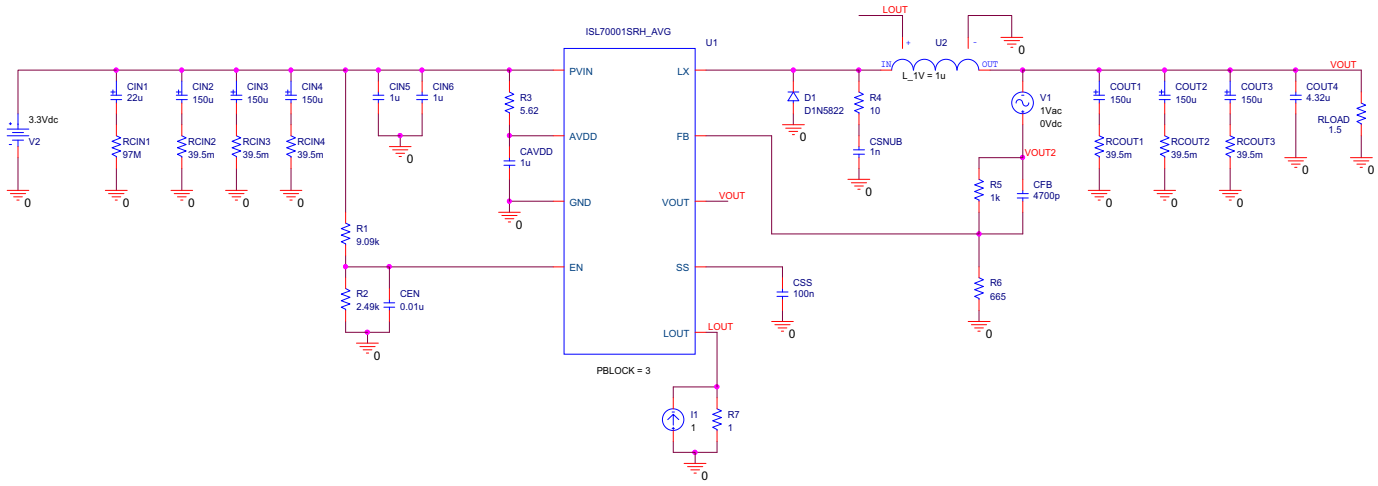

FIGURE 1. BASIC NONINVERTING GAIN CONFIGURATION IN ORCAD SPICE FOR AC ANALYSIS

Power Blocks

The model has a parameter named PBLOCK, which is equivalent to the number of LX nodes connected on the ISL70001SRH in a given application. By double clicking the text you can modify the number of blocks to match the prototype board.

Inductor Value

The average model is based on a mathematical representation of the ISL70001SRH. The value of the inductor is needed for the model to accurately simulate the regulator. The model has an added pin LOUT, which is connected to a current source I1 and resistor R_7. These create a voltage that is fed into the pin and into the inductor U2. U2 translates the voltage into inductance by the equation L_1V = 1µ, for every volt on LOUT the inductor value is 1µH. To change the inductor value to say for example 500nH, one must change R_7 to 0.5Ω.

V_{OUT} Value

The output voltage must also be known for the average model to work correctly. The VOUT pin is added to read the output voltage and feed into the internal equations within the ISL70001SRH model. For proper simulation of the model V_{OUT} must be connected to the output voltage of the ISL70001SRH application schematic.

Simulation Performance Curves

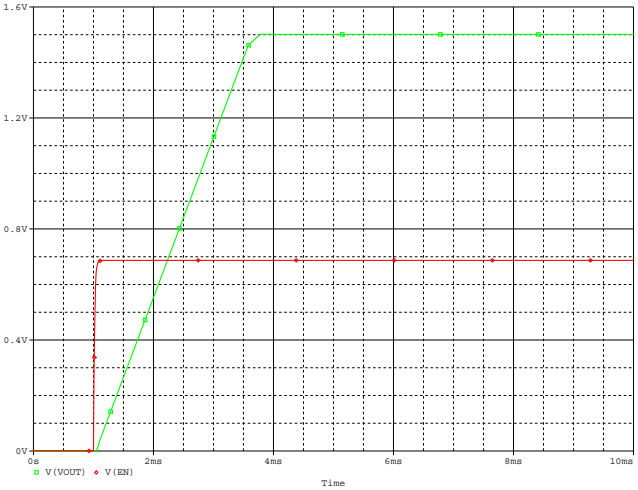

FIGURE 2. SIMULATED START-UP

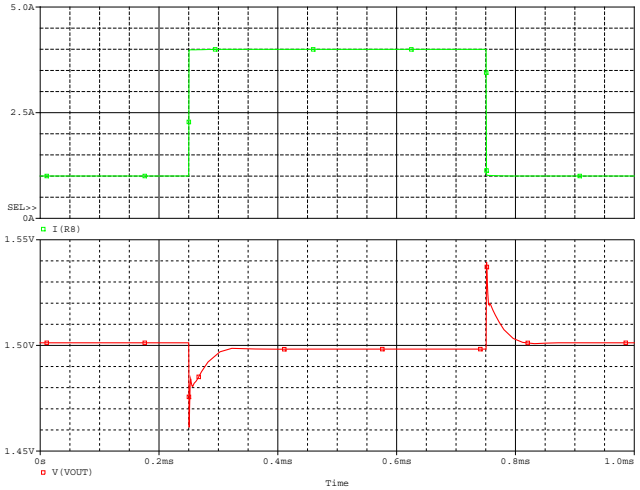

FIGURE 3. SIMULATED 3A TRANSIENT RESPONSE

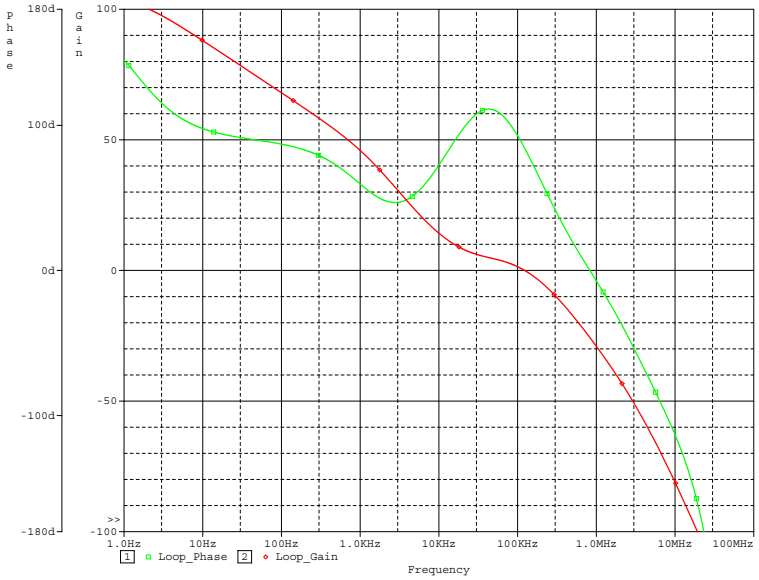

FIGURE 4. SIMULATED LOOP RESPONSE